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Temperature dependence of electrical characteristics and interface state densities of Au/n-type Si structures with SnS doped PVC interface

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Abstract

In this study, the electrical properties of Au/(SnS doped PVC)/*n*–Si structures were investigated in detail using current/voltage (*IV*) data in wide temperature range (80–340 K by 20 K steps). Some of the basic electrical parameters such as ideality factor (n), saturation current (I_0), and barrier height (Φ_{bo}) were obtained. When these parameters were extracted using thermionic emission (TE) theory, it was found that the value of n decreases whereas Φ_{bo} increases with increasing temperature. This result can be explained by the barrier height (BH) inhomogeneity. The observed two linear regions in the plots of Φ_{bo}–n, Φ_{bo}–$(1/2kT)^1$ and $(n^{-1}$–$1)$–$(1/2kT)$ in temperature regions of 80–160 K and 80–340 K form an evidence to the presence of Double Gaussian distribution (DGD). Using the plot of Φ_{bo}–$(1/2kT)$, the values of mean BH ($\bar{\Phi}_{bo}$) and standard deviation (σ_S) were found as 0.486 eV and 66 mV for first region, and 0.984 eV and 139 mV for second region, respectively. Thus, the effective Richardson constant (A^*) was obtained using the interception point of the modified Richardson plot for these regions as 7.013×10^{-6} A.K^{-2}cm^{-2} and 88.12 A.K^{-2}cm^{-2}, respectively. It is clear that A^* value for second region is closer to theoretical value (=112 A.K^{-2}cm^{-2} for *n*–Si). Finally, the energy dependent profile of the surface-states (N_{ss}) was extracted using Card-Rhoderick method and N_{ss} was found to range from $\sim 10^{12}$ (at 80 K) to 10^{13} eV^{-1} cm^{-2} (at 340 K).

Introduction

Silicon is a group IV semiconductor in the periodic table, and is one of the most important semiconductors known advantageously for powerful devices from electronic technology [1–12]. Among the electronic devices based on Si semiconductor, metal-semiconductor (MS) and metal-insulator-semiconductor (MIS) type electronic structures have been studied tremendously because of their unique electrical, optical and structural features where interfacial layer's homogeneity and thickness play a critical role in the performance, cost, and stability of these structures [13–15]. Today, the main scientific and technical problems of these structures are associated with the performance improvement, cost reduction, getting more accurate and reliable results on the conduction mechanism (CM) and nature of BH at M/S interface. Therefore, researchers start to use a polymer interlayer due to its high surface area to volume rate, light weight, good mechanical strength, charge storage capacity, flexibility, high dielectric strength, and easy processing techniques including electrospinning, solid-liquid phase separation and template synthesis.

A conventional insulator layer (SiO_2) formed on a semiconductor surface via traditional methods such as thermal-oxidation cannot completely passivate the active dangling bonds at the semiconductor surface. In addition, it leads to an increase in the leakage current. Therefore, in recent years, many researchers purpose

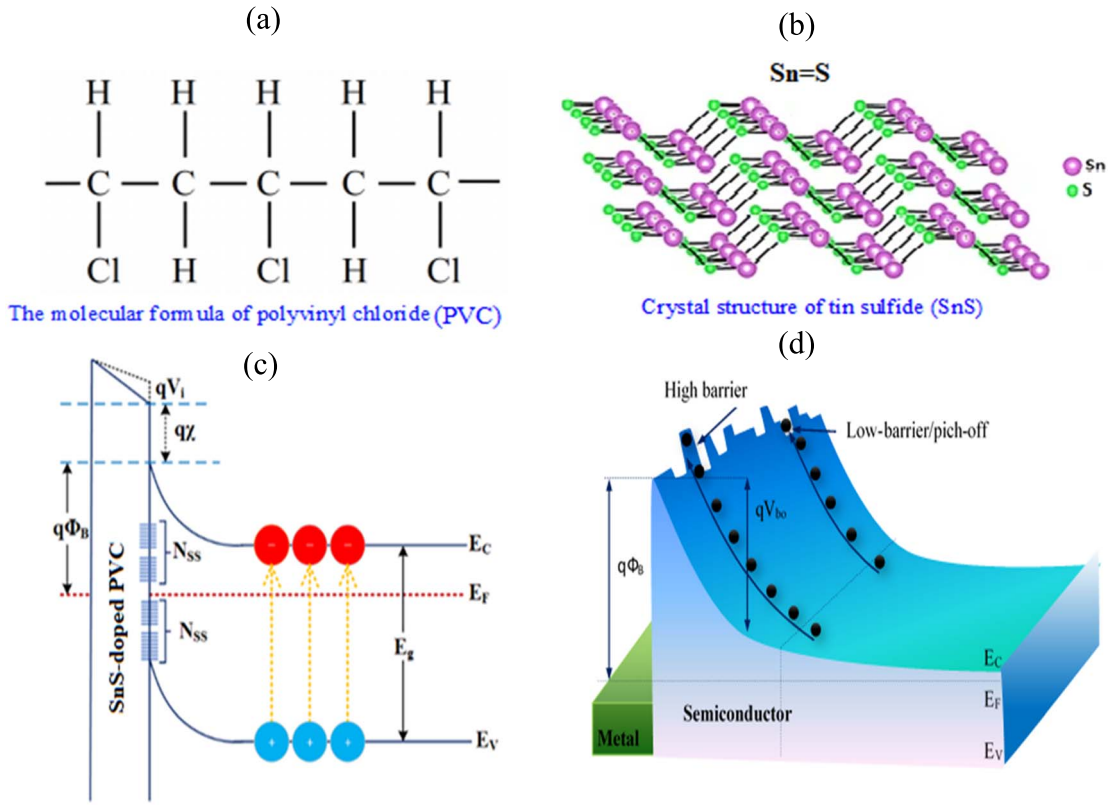

Figure 1. (a) The molecular formula of polyvinyl chloride, (b) crystal structure of tin sulfide, (c) energy-band diagram of the MPS or MIS type structures, and (d) schematic diagram of MS structure with barrier inhomogeneities.

improving the electrical and dielectric properties of these structures and for this purpose they start to use a polymer interlayer due to its high surface-area to volume-rate, light weight, good mechanical-strength, charge storage-capacity, flexibility, high dielectric strength, and easy processing techniques such as electrospinning, solid-liquid phase separation and template synthesis [4–9]. Although, polymers/organics have low conductivity and dielectric, they can be obtained by doping appropriate metals or metal-oxides into the polymers. For example, Altındal-Yerişkin *et al* [9] were investigated the effects of (Graphene doped-PVA) interlayer on the determinative electrical parameters by using Au/(0.07 Gr-PVA)/*n*–Si (MPS) with several graphene concentrations (%1,3,5,7,10), and they were found that the RR($I_{forward}/I_{reverse}$) value of MPS structure is 493 times higher than RR value of MS structure and the values of interface-states/traps (N_{SS}) of polymer-semiconductor (MPS) structures were found 92.98 lower than these values of MS structure for %7 concentration of graphene. Thus, Au/(SnS-doped PVC)/*n*–Si MPS structures are effectively utilized in various applications due to their favorable properties. For these type of structures, controlling interface properties is critical in device applications. Moreover, reliability and performance of these structures are dependent on the processing of surface, the density of N_{SS}, electric field and series resistances (R_S). MPS structures have a lot of advantages compared to MS or MIS type. Therefore, a complete description of conduction mechanism through barrier and understanding of the formation/nature of BH also still remain a challenging problem especially at low temperatures. This is because the analysis of the conduction mechanism in these devices based on standard TE theory usually reveals an increase in n and a decrease in BH with decreasing temperature and also conventional Richardson plot deviates from linearity and yields very low Richardson constant (A^*) compared to its theoretical value [16–21].

Tin sulfide with the chemical formula SnS is a chemical compound of tin and sulfur. SnS is one of the most important semiconductors from the Periodic table's IV–VI groups. Also, tin and sulfur compounds are plentiful and environmentally friendly. These favorable properties of tin sulfide have led to the development of thin tin sulfide films for semiconductor applications [22–24]. Figure 1(a) shows the molecular formula for polyvinyl chloride (PVC) very inexpensive polymer with appropriate chemical properties for usage as a membrane material. Due to the adhesion of organic molecules to the membrane's surface fouling of the membrane pores is caused by hydrophobic PVC polymers. Therefore, many promising results of SnS production aroused curiosity and its applications in photovoltaic cells (PVC) became an important study topic. In this study, the molecular structures of tin sulfide (SnS) and crystal structure of tin sulfide used for MS interface are shown in

figures 1(a), (b), respectively. Thus, the MS structures with SnS-doped PVC interface have gained interest because of their electrical and optical characteristics in prospect of creating micro and nanostructures that may be employed as active materials in electronic devices [13–15, 23, 24]. The energy-band diagram of the MPS or MIS type structures is given in figure 1(c). As shown in figure 1(c), electrical characteristics of the MPS or MIS type structures depend on many factor such as the existence of barrier homogeneity and interlayer at M/S interface, surface states (N_{SS}) located at between interlayer/semiconductor interface, temperature, voltage, doping-level of donor/acceptor atoms, series-resistance (R_S). Among them, N_{SS} are located in the forbidden bandgap (E_g) at junction and they act as recombination centers which can release or capture many electrons. They usually stem from the unsaturated dangling-bonds of the surface atoms and organic contaminations in laboratory environment, oxygen vacancies, and some periodic disorders. In addition, as shown in figure 1(d), the existence of barrier inhomogeneity at M/S interface was included lower barriers/patches or pinch-off around mean BH so it is indeed effective on the conductance mechanisms. At low temperatures, carriers with low energy can easily pass through these patches and hence lead to an increase in the current or ideality factor. However, at room temperature or above, the lower BH patches at interface are offset by the much greater area of the uniform region, as a result, most current flows through the uniform region rather than patches.

In the literature, there are some experimental studies on SnS and PVC interfacial layer at room temperature. However, there is not much information on the conduction mechanism (CM) of Au/(SnS-doped PVC)/*n*–Si structures in wide temperature range. Guo *et al* [14] focused on the synthesis of multi-structured SnS nanocrystals for increasing performance of photovoltaic devices. Demirezen *et al* [24] have also studied the effect of (Mo-doped PVC + TCNQ) interlayer on the electrical characteristics in the Au/(PVC + TCNQ)/p–Si devices at room temperature. Bronusiene *et al* [25] investigated the effect of ascorbic acid on the properties of tin sulfide films for supercapacitor application. Yücedağ *et al* [24] investigated dielectric properties and ac electrical conductivity of the Au/(PVC + TCNQ)/p–Si structures both as function of temperature and voltage. Although many more similar works can be given, there are not sufficient number of works on these structures regarding their characteristics in wide temperature range. Furthermore, analysis of the *IV* measurements of these devices at only room temperature regime cannot supply detailed information on interface properties, CMs, and nature of BH at junction compared to the analysis performed in wide temperature range.

Therefore, the *IV* measurements of Au rectifier contacts on *n*-type Si structure with SnS-doped PVC interface were carried out in the wide temperature range (80–340 K) for detailed information on the electrical properties and surface states. The first goal is to fabricate Au/(SnS-doped PVC)/n type Si (MPS) structures. The second goal is to investigate basic electrical parameters such as *n*, RR, I_0 and barrier height (Φ_{bo}) of this structure and their dependence on temperature using the *IV* data in the wide range of temperature and voltage. The third goal is to obtain BH and A^* values for different temperature regions considering the presence of DGD of the barrier inhomogeneity. The fourth goal is to compare the electrical characteristics obtained from Norde's theory and TE theory. The last goal is to extract the energy (E_C–E_{SS}) dependent profile of N_{SS} for each temperature by using Card-Rhoderick method. Therefore, the Au/(SnS doped PVC)/n–Si structure can be successfully explained by the double GD of BH around BH, and furthermore, (SnS-doped PVC) thin organic interfacial layer at Au/n–Si interface can be improvement of the performance of Au/n–Si structure in terms of low values of Nss and leakage current and high values of BH and RR through passivation. This means that the value of n decreases whereas Φ_{bo} increases with increasing temperature and such behavior of them was successfully explained by the barrier inhomogeneity. The observed two linear regions of the Φ_{bo}-*n* and Φ_{bo} - $(1/2kT)^1$ in temperature regions of 80–160 K and 80–40 K form an evidence to the presence of Double Gaussian distribution (DGD). Thus the obtained value of effective Richardson constant (A^*) was obtained from the modified Richardson plot for these regions as 7.013×10^{-6} A.K^{-2}cm^{-2} and 88.12 A.K^{-2}cm^{-2}, respectively. It is clear that A^* value for second region is closer to theoretical value (=112 A.K^{-2}cm^{-2} for *n*–Si). The values of N_{ss} was extracted from Card-Rhoderick method and they changed from ~10^{12} (at 80 K) to 10^{13} eV^{-1} cm^{-2} (at 340 K) which are suitable for similar devices".

Experimental procedures

Fabrication of the Au/(SnS-doped PVC)/n–Si (MPS) structures

Before the fabrication processes, *n*–Si (100) wafer with 10–20 Ω-cm resistivity, 525 μm thickness and 4.3×10^{15} cm^{-3} concentration of phosphor atoms was chemically cleaned by using RCA (Silicon Wafer Cleaning) cleaning procedure. After surface cleaning of *n*–Si wafer, highly pure (0.999) gold metal was thermally grown on the whole back side wafer at 4×10^{-6} Torr by using VAKSIS thermal evaporation system (TES) and then n–Si/Au wafer was annealed at 570 °C for 3 min in N_2 (Nitrogen) atmosphere to get a good ohmic contact. After, the front surface of n–Si wafer was coated with 'as prepared' solution of PVC + SnS (1:1) solutions in THF by spin coating method with 3000 rpm for 1.0 min. Finally, rectifier contacts were formed onto (SnS-doped PVC) film

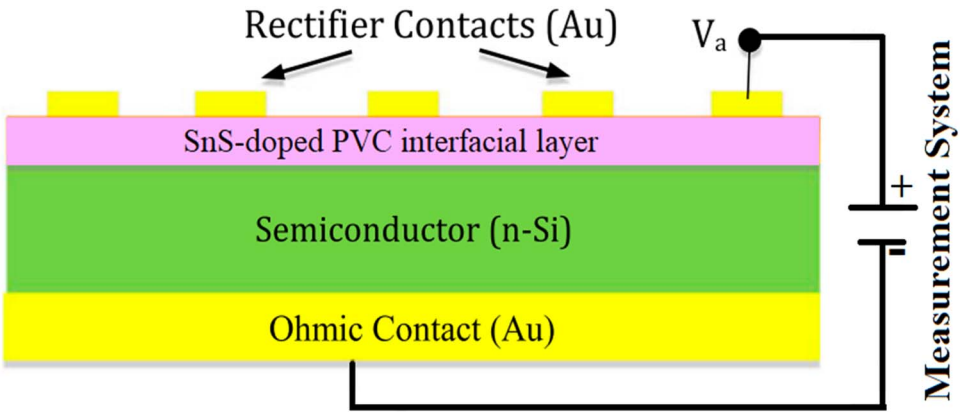

Figure 2. The schematic diagram of the Au/SnS-doped PVC/*n*–Si structure.

layer with 50 nm thickness and 1 mm diameter in the same TES. The temperature dependent *IV* measurements were performed by using a Keithley 2400 Source-Meter, a Janis VPF-475 cryostat, and a Lake-Shore-331 temperature controller with the help of a computer through an IEEE- 488 AC/DC converter card. The molecular structure of the (SnS-doped PVC), schematic-diagram of the Au/(SnS-doped PVC)/*n*–Si structures, and the setup of measurement system were represented in figures 1, 2, and 3, respectively.

Preparation of tin sulfide (SnS) solution

The structures of tin Sulfide (SnS) have been prepared by the tin chloride ($SnCl_2$) and sodium sulfide (Na_2S) provided by Sigma-Aldrich and Merk (German companies) precursors. To synthesize tin sulfide nanostructure, first, a 0.2 M solution of tin chloride ($SnCl_2$) and a 1 M solution of sodium sulfide (Na_2S) must be prepared. To do this, 0.76 g and 2.64 g of tin chloride and sodium sulfide were respectively solved into 20 ml of deionized water. Next, the solution of sodium sulfide (Na_2S) was added dropwise to the tin chloride ($SnCl_2$) solution upon the magnetic stirrer for 15 min. Then, the resulting mixture was put in an autoclave at 160 °C for 22 h. Finally, the obtained production had been rinsed 4 times by ethanol (C_2H_5OH) and was dried at 50 °C for 10 h.

Preparation of polyvinylchloride (PVC) solution

Low molecular-weight poly-(vinyl chloride) (PVC) with 48,000 molecular weight, K-value of 55–57, and density of 1.4 g ml at 25 °C as white-color fine powder was purchased from Sigma-Aldrich and Tetrahydro-furan (THF) was purchased from Merck. For preparation of SnS-PVC nanocomposite materials in THF in the first step 0.34 g PVC powder and 0.34 g of SnS powder were mixed ın 30 ml THF solution in a flask under magnetic stirrer on hot plate at 20 °C for 30 min.

Results and discussions

Figure 4 shows the current-voltage-temperature (*I*–*V*–*T*) curves of the Au/SnS-doped PVC/*n*–Si structure in wide temperature range (80 K–340 K). As seen in figure 4, both reverse and forward current increase with the increase in temperature and this indicates strong rectification properties of the Au/SnS-doped PVC/*n*–Si structure. However, *I*–*V*–*T* curves deviate from linearity due to increasing effects of R_s and interfacial organic layer at high-forward voltages. The values of n, Φ_{bo}, I_0, rectification ratio ($RR = I_F/I_R$ at ±V), and R_S of the Au/SnS-doped PVC/*n*–Si structure were derived from the *I*–*V*–*T* measurements. According to thermionic emission (TE) theory, the *IV* relations of Au/SnS-doped PVC/*n*–Si structure at forward bias voltage (V_F) can be expressed by [1, 2, 19–24, 26–31];

$$I = I_0 \exp\left(\frac{q(V_F - IR_S)}{nkT}\right)\left[1 - \exp\left(\frac{-q(V_F - IR_S)}{kT}\right)\right] \quad (1)$$

where q is charge of an electron ($=1.6 \times 10^{-19}$ C), k is the Boltzmann's constant ($=1.3806 \times 10^{-23}$ J K^{-1}), R_S is series resistance, and IR_s is the voltage drop due the R_s structure. Using intercept point of the linear regime of the *LnI* versus V_F curves in figure 4, we obtained the saturated currents (I_0) from $I_0 = 2.988 \times 10^{-8}$ A to $I_0 = 1.265 \times 10^{-5}$ A in the temperature range of 80–340 K. Thus, barrier height (Φ_{bo}) can be extracted using I_0 values in following expression;

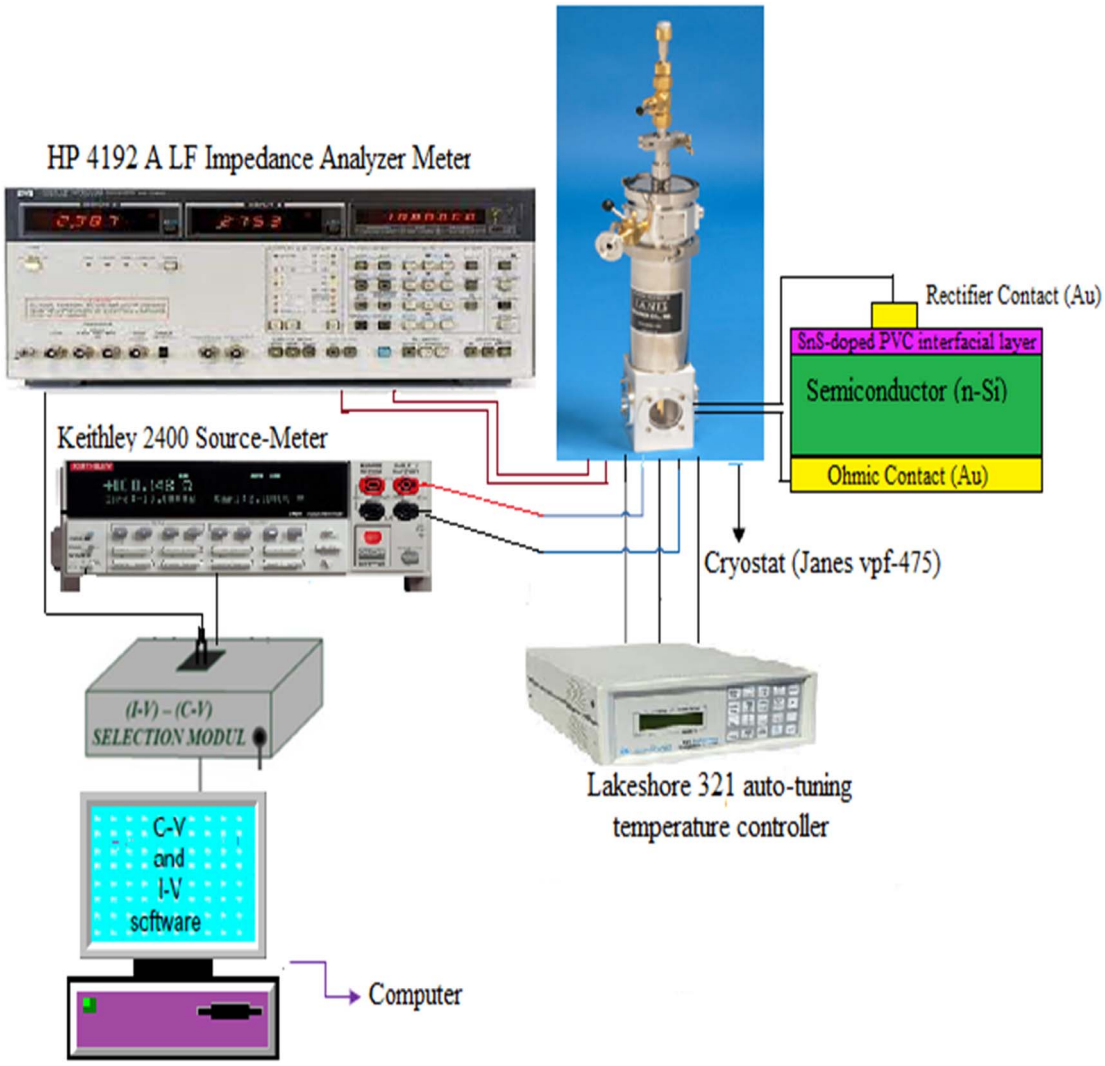

Figure 3. The schematic diagram of Au/SnS-doped PVC/*n*–Si structure and *I–C–V* measurement system.

$$I_o = AA^*T^2 \exp\left(-\frac{q\Phi_{bo}}{kT}\right) \tag{2}$$

where A and A* are the contact area (=7.85 × 10^{-3} cm^2) and Richardson constant ($A^* = 112$ A $cm^{-2}K^2$ for *p*-type Si), respectively. The *n* and Φ_{bo} values were also obtained by using slope and intercept values of *LnI* versus V_F curves for each temperature in following expressions, respectively;

$$n = \left(\frac{q}{kT}\right)\left(\frac{dV_F}{d\ln I}\right) \tag{3}$$

and

$$\Phi_{bo} = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_o}\right) \tag{4}$$

Obtained experimental values of the *n* and Φ_{bo} for Au/(SnS-doped PVC)/*n*-Si structure varies from 0.179 eV and 11.74 for 80 K to 0.669 eV and 4.77 for 340 K, respectively. In addition, the values of the ideality factor and barrier height calculated for each temperature were tabulated in table 1 and also shown in figure 5. The barrier height and ideality factor values were obtained in the voltage range of 0.299–0.723V from the $\ln(I_F)$–V_F curves. As seen in figure5 and table 1, the value of *n* decreases, while the value of Φ_{bo} increases with increasing temperature in the range of 80–340 K. Such increase in BH with increasing temperature especially at low temperatures is not in agreement with the negative temperature coefficient of the E_g or BH for ideal SDs (a = dE_g/dT which is equal to -4.73×10^{-4}eV.K^{-1}). Therefore, the investigating the possible conduction mechanisms at low temperatures is more important to get more accuracy and reliable results on the conduction mechanisms, basic electrical properties, and the nature of BH at M/S interface in wide range temperature. The reason for an increase in the Φ_{bo} and a decrease in *n* factor with increasing temperature is associated with the

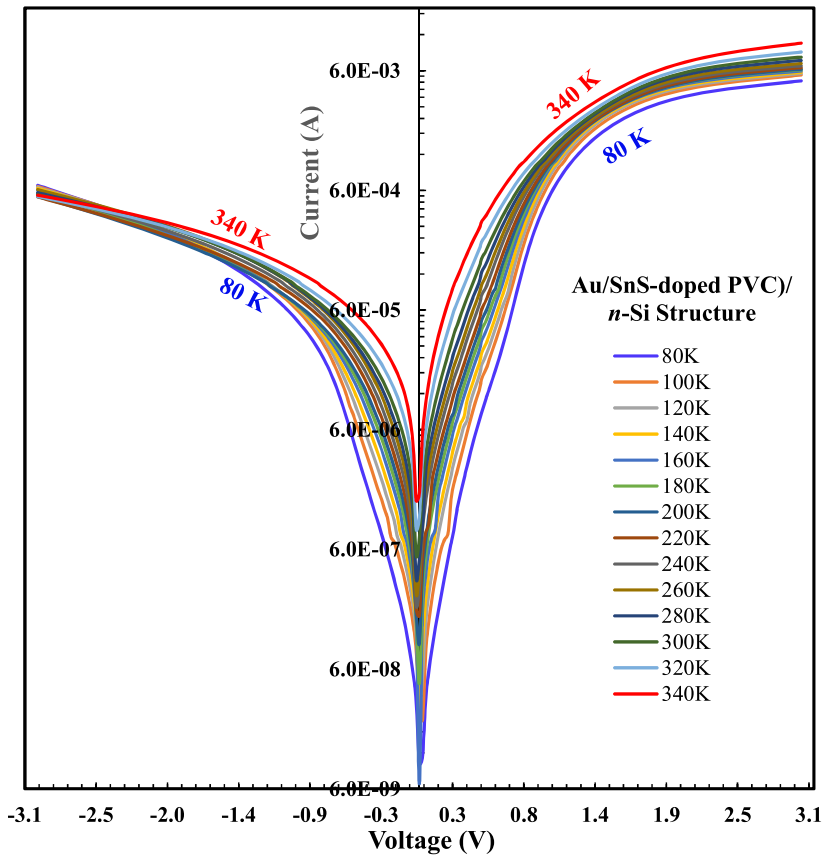

Figure 4. Experimental reverse and forward bias current–voltage curves of the Au/SnS-doped PVC/*n*–Si structure in the temperature range of 80–420 K.

Table 1. The main electrical parameters f of or the Au/SnS-doped PVC/*n*–Si structure obtained from *I*–*V* measurements.

T (K)	*n I*–*V*	Φ_b (*eV*) *I*–*V*	Rectification ratio for ± 1.0 V	Rectification ratio for ± 2.0 V	Rectification ratio for ± 3.0 V	Φ_b (eV) Norde	$R_S(\Omega)$ Norde
80	11.742	0.179	8.83	12.91	7.42	0.207	9504.13
100	10.240	0.219	9.49	14.28	8.48	0.252	5901.87
120	9.380	0.259	10.25	15.04	8.84	0.292	3520.41
140	8.388	0.301	11.15	15.72	9.27	0.336	2959.56
160	7.326	0.343	11.80	16.60	9.89	0.382	2338.98
180	7.147	0.382	12.36	17.72	10.71	0.422	2011.01
200	6.668	0.423	12.56	18.62	11.55	0.464	1756.62
220	6.253	0.462	11.73	18.22	11.95	0.506	1489.40
240	5.831	0.501	11.48	17.26	11.65	0.547	1209.11
260	5.385	0.541	10.98	16.23	11.23	0.590	1019.32
280	5.101	0.578	11.56	17.41	12.65	0.630	838.54
300	4.889	0.613	11.83	18.37	14.04	0.665	625.00
320	4.831	0.643	12.16	19.60	16.04	0.693	415.66
340	4.774	0.669	12.22	20.50	18.52	0.719	258.55

inhomogeneous nature of the interface and BH of the Au/SnS-doped PVC/*n*-Si structure [11, 32, 33]. According to Tung [32], such behavior of Φ_{bo} and *n* with temperature is the result of existence of locally irregular lower barriers or pinch-offs with respect to the mean BH at M/S interface. However, according to Werner and Guttler [11], BH should generally be distributed according to the Gaussian function distribution which will provide a significant temperature and voltage dependent BH. At the time same, the presence of (SnS-doped PVC) thin interlayer at Au/n–Si interface may also cause the inhomogeneity of BH. In fact, this interface layer may also affect the current conduction between Au and *n*–Si semiconductor. Furthermore, because current transport across the MS, MIS, and MPS structures is dependent on temperature and voltage, hence electrons cause a current to flow through the barrier, they can go through the high barriers at higher temperatures and the low barriers at lower temperatures [11, 32–37].

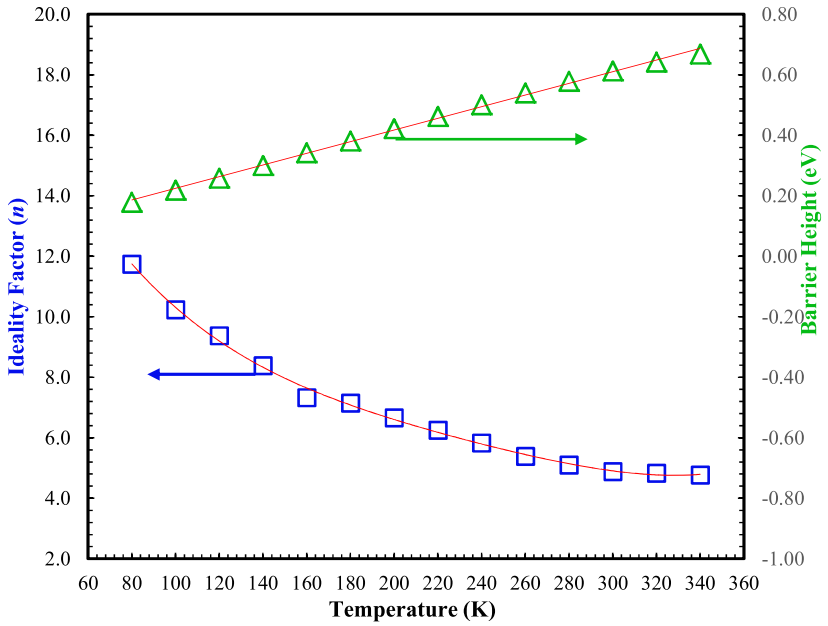

Figure 5. Barrier height versus temperature and ideality factor versus temperature curves of the Au/SnS-doped PVC/*n*–Si structure obtained from forward bias *I*–*V* data.

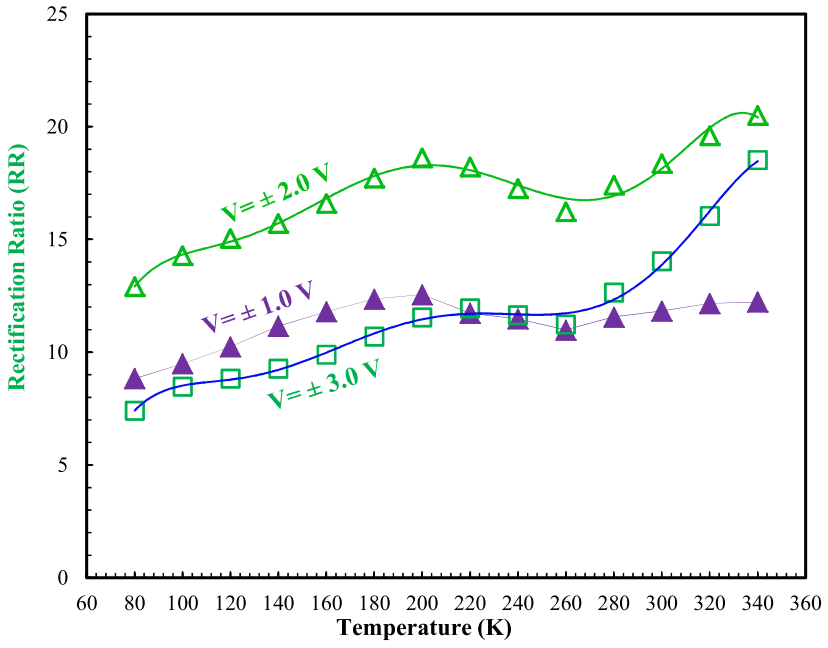

Figure 6. Temperature dependence of rectifying ratio of the Au/SnS-doped PVC/*n*–Si structure for potential ranges ±1.0 V, ±2.0 V and ±3.0 V.

Another important parameter that reflects performance of these structures is *RR*. It is the proportion of current values flowing at the same voltage but in opposite bias directions. Thus, rectification ratio can be written as $RR = I_F/I_R$ = Forward current/Reverse current at a certain bias voltage. As seen in figure 6 and table 1, the rectification ratio values obtained in the range of 80–340 K at ±1.0 V, ±2.0 V and ±3.0 V for the Au/SnS-doped PVC/n–Si structure increase with increasing temperature. According to figure 6 and table 1, the values of RR change with the temperature and also increases with increasing temperature at ±1.0 V, ±2.0 V and ±3.0 V. However, the RR values for ±2.0 V are higher than values obtained for ±1.0 V and ± 3.0 V and this result can be attributed to effect of R_s at high voltages. Likewise, the RR values are low owing to the forward and reverse currents are close to each other at low voltages (at ±1.0 V).

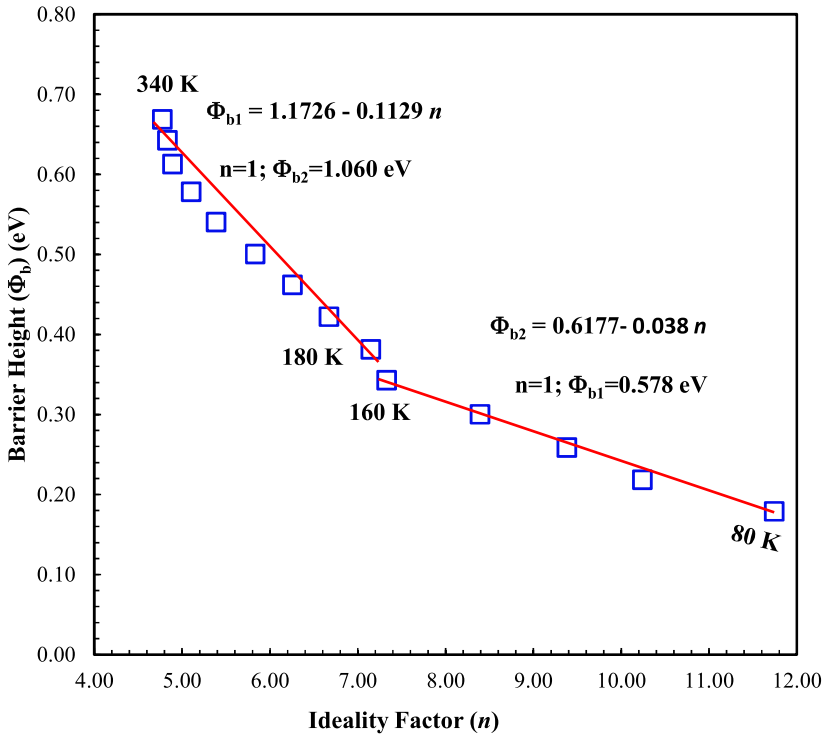

Figure 7. The plot of barrier height versus ideality factor versus temperature the Au/SnS-doped PVC/*n*–Si structure at various temperatures.

Figure 7 shows the graph of Φ_{bo} versus n for the Au/SnS-doped PVC/*n*–Si structure between the 80 K and 340 K. This plot reflects the quality of the interface and suggests that these two parameters are related linearly for two temperature regions that will be called low temperature region (from 80 K to 160 K) and high temperature region (from 180 K to 340 K). The existence of two different linear regions in figure 7 indicates the existence GD of BH. For Au/SnS-doped PVC/*n*–Si structure, the extrapolation Φ_{bo} values yields Φ_{bo} values for the case of $n = 1$ as 1.060 eV and 0.578 eV for the high temperature and low temperature regions, respectively. The barrier height value found for high temperature region is very close to the band gap of Si, while the one found for low temperature region is lower than the known the band gap of Si. Therefore, varying barrier height values for different temperature regions are associated with lateral barrier inhomogeneity at the metal semiconductor interface [37–39]. This instance demonstrates that thermionic emission (TE) controls current transport at temperatures over 180 K, whereas thermionic field emission (TFE) controls current transport at temperatures below 160 K [1, 2, 40–42]. The plot of nkT versus kT of Au/SnS-doped PVC/*n*–Si structure was given in figure 8 for a better understanding of current mechanism. TE is predominant when $E_{oo} \approx kT/q$ whereas field emission (FE) or TFE is not predominant when $E_{oo} \approx kT/q$. Thus, for FE to be dominant, E_{oo} or nT should be almost constant at each temperature. Here, E_{00} is the equivalent energy of the carrier concentration. Because, pure TE occurs for an ideal structure and the values of ideality factor does not change with increasing temperature (for y = x curve in figure 8). The plot of nkT versus kT of Au/SnS-doped PVC/*n*–Si structure revealed a nearly parallel but not precisely parallel line to the ideal device (for nkT versus kT plot). Furthermore, this case can also attributed to the inhomogeneity of BH at Au/n–Si interface [43–45].

As explained above, BH of MS, MIS or MPS structures may exhibit double Gaussian distribution (GD). That is, if the barrier has a GD, its values over the Schottky contact area are expressed in terms of the mean BH ($\bar{\Phi}_{bo}$) and σ_o which is a measure of the homogeneity of the barrier. Moreover, the reduction in BH with a decrease in temperature is associated the lateral distribution of BH. The total current in a forward bias V is then calculated as follows;

$$I(V_F) = I_0 \exp\left(\frac{qV_F}{n_{ap}kT}\right)\left[1 - \exp\left(-\frac{qV_F}{kT}\right)\right] \tag{5}$$

with

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{ap}}{kT}\right) \tag{6}$$

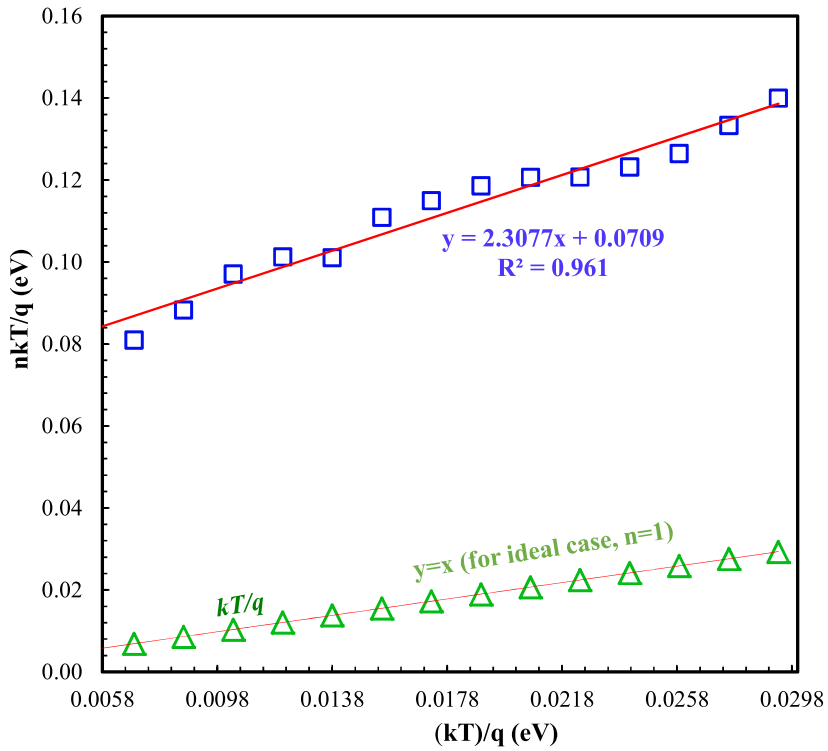

Figure 8. The plot of *nkT/q* versus *kT/q* of Au/SnS-doped PVC/*n*–Si structure.

where Φ_{ap} and n_{ap} are the apparent BH and *n*, respectively, which are given by

$$\Phi_{ap} = -\frac{q\sigma_o^2}{2kT} + \bar{\Phi}_{bo} \tag{7}$$

$$\left(\frac{1}{n_{ap}} - 1\right) = \rho_2 - \frac{q\rho_3}{2kT}. \tag{8}$$

where ρ_2 and ρ_3 are dimensionless voltage coefficients as well as the barrier height distribution's deformation voltage values. Therefore, the plots of Φ_{ap}-$(2kT)^{-1}$ and $(n_{ap}^{-1} - 1)$–$(2kT)^{-1}$ are shown in figure 9 and these two plots also have two distinct linear regions with different slope and intercept values just like the plot of Φ_{ap}—n (figure 7).

As shown in figure 9, the values of the σ_o and $\bar{\Phi}_{bo}$ are calculated by using the slope and intercept values in equation (7) as 139 mV and 0.984 eV, respectively, for high temperature region (180–340 K). The results are 66 mV and 0.486 eV, respectively, for low temperature region (80–160 K). Similarly, the values of ρ_2 and ρ_3 are obtained using equation (8) as 0.702 eV and 0.005 eV for high temperature region (180–340 K) and 0.823 eV and 0.0013 eV for low temperature region (80–160 K) , respectively. The experimental results show that smaller ρ_2 and larger ρ_3 voltage deformation-coefficients points out a wider and greater BH distribution for high temperature region (180–340 K) compared to than low temperature region (80–160 K). The double GD behavior was also reported by other studies [46–49].

In other words, FE and TFE theories cannot explain the greater n values at lower temperatures. Thus, FE and TFE theories can only be described in terms of metal-to-semiconductor barrier inhomogeneity. According to Tung [32, 33, 50], the large value of ideality factor (*n*) and its linearity versus $(kT)^{-1}$ can also constitute strong evidence of an inhomogeneous BH. The plot of $\ln(I_o/T^2)$ versus $(kT)^{-1}$ is a helpful plot for obtaining the values of effective barrier height (Φ_{bo}) and effective Richardson constant (A^*). Therefore, equation (2) can be rearranged as following for the plot of $\ln(I_o/T^2)$ versus $(kT)^{-1}$;

$$\ln\left(\frac{I_o}{T^2}\right) = -\frac{q\Phi_{bo}}{nkT} + \ln(AA^*) \tag{9}$$

Figure 10 shows the plots of $\ln(I_o/T^2)$ versus $(nkT)^{-1}$ or $(kT)^{-1}$. According to equation (9) and figure 10, the plot of $\ln(I_o/T^2)$ versus $(nkT)^{-1}$ exhibits linear behavior for whole temperature range whereas the plot of $\ln(I_o/T^2)$ versus $(kT)^{-1}$ shows linearity only for high temperature region. The nonlinearity of the plot of $\ln(I_o/T^2)$ versus $(kT)^{-1}$ for low temperature region is due to recombination in the depletion region. Thus, according to

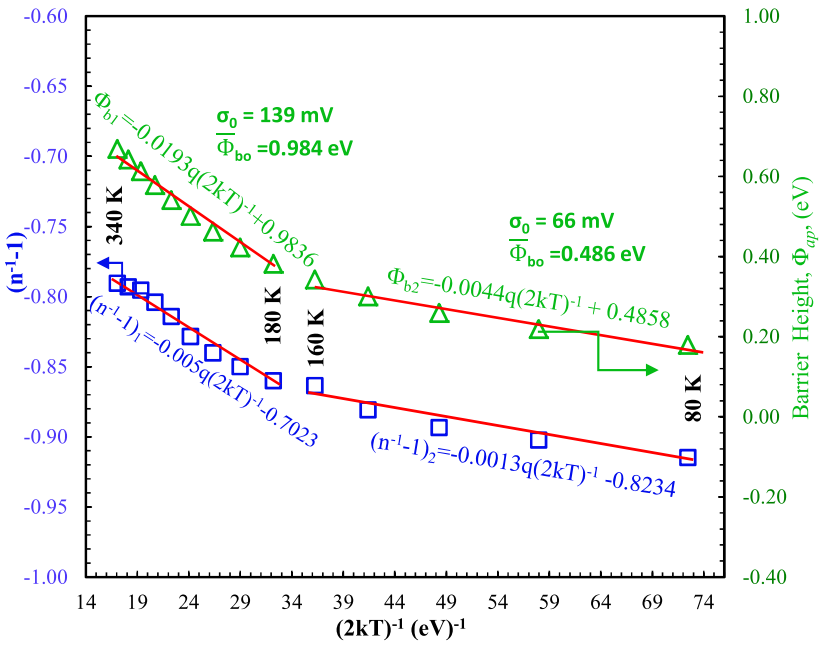

Figure 9. The plots of Φ_{ap} (open triangles) versus $(2\,kT)^{-1}$ and of $(n_{ap}^{-1} - 1)$ (open squares) versus $(2\,kT)^{-1}$ of Au/SnS-doped PVC/*n*–Si structure according to Gaussian distribution of BH.

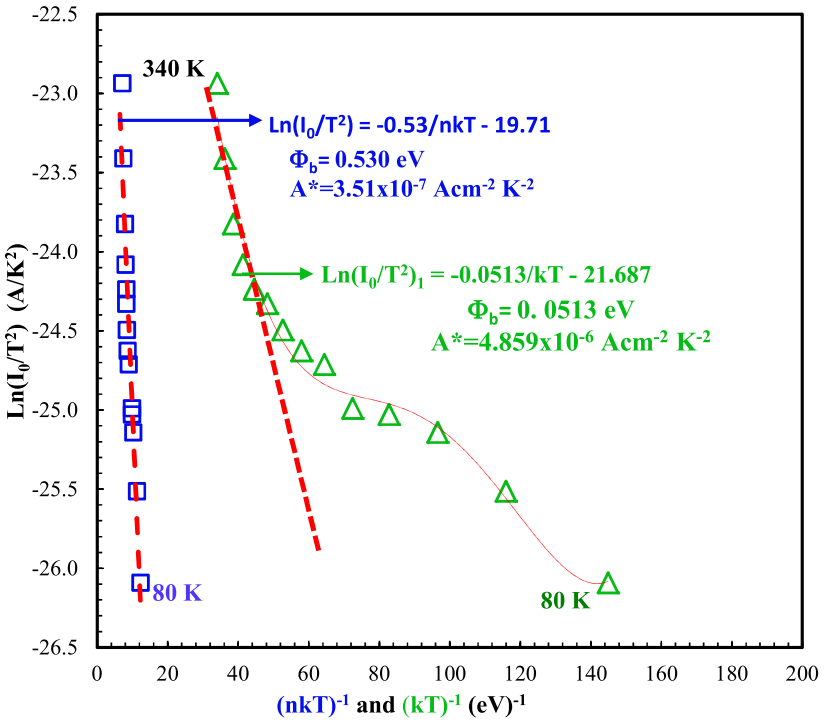

Figure 10. Conventional activation energy ($\ln(I_0/T^2)$ versus q/kT) plot (open triangles) and ($\ln(I_0/T^2)$ versus q/nkT) plot (open squares) of the Au/SnS-doped PVC/*n*–Si structure.

equation (9), the slope and y-intercept of the plot of $\ln(I_o/T^2)$-(q/nkT) give the values of Φ_{bo} and A^*, respectively. The values of $\bar{\Phi}_{bo}$ and A^* were found as 0.530 eV and 3.51×10^{-7} A/(cm^2 K^2), respectively, using the plot of $\ln(I_o/T^2)$-(q/nkT). However, the values of activation energy ($E_a = \Phi_{bo}$) and A^* were found as 0.0513 eV and 4.86×10^{-6} A/(cm^2 K^2), respectively, for the plot of $\ln(I_o/T^2)$-(q/kT). Clearly these values of A^* are quite lower than the theoretical value of 112 A cm^{-2} K^{-2} for the conduction band (electrons) of n–Si [1, 2]. The reason for this deviation in A^* values can be attributed to BH inhomogeneity and potential fluctuations at the

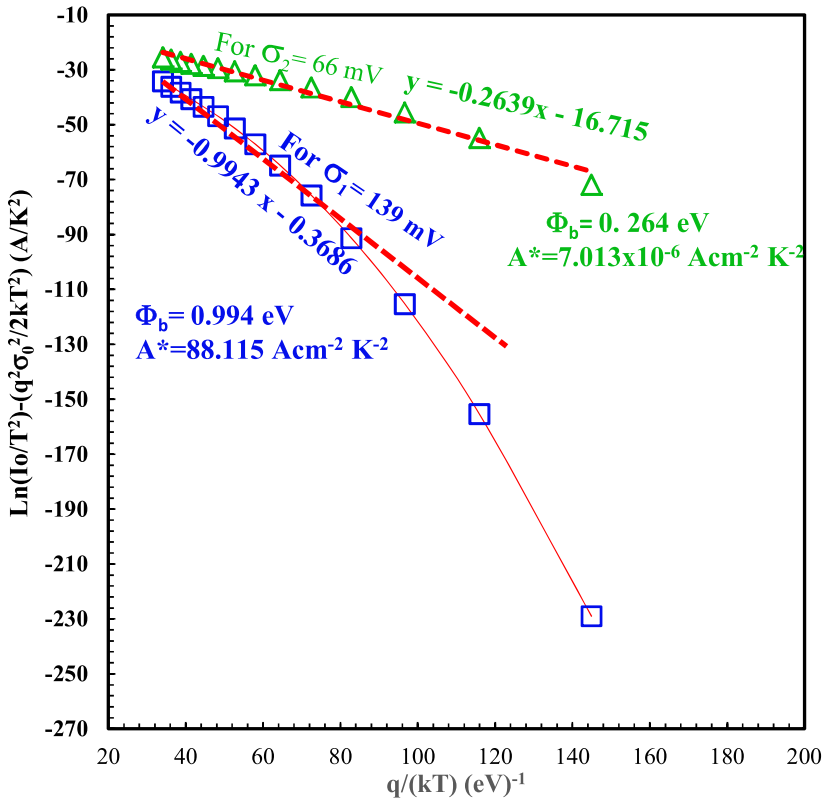

Figure 11. Modified activation energy ($\ln(I_0/T^2)$—$q^2\sigma_o^2/2k^2T$ versus q/kT) plots of the Au/SnS-doped PVC/*n*–Si structure according to double Gaussian distribution of BH.

interface consisting of low and high barrier patches [51–54]. Also, Horvath [55] explained that low values of A^* may stem from the lateral inhomogeneity of the barrier.

Hence, the mean values of BH and A^* were obtained using the modified-Richardson plots. For this purpose, equations (7) and (9) are rewritten as below by taking into account the GD of BH and the modified Richardson or activation-energy plot [32, 33];

$$\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_0^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\bar{\Phi}_{bo}}{kT} \tag{10}$$

where $\bar{\Phi}_{bo}$ is the mean value of BH and other terms were defined above. Figure 11 shows the plot of $\ln(I_0/T^2)$-$q^2\sigma_o^2/2k^2T^2$ versus (q/kT) which is known as the modified-Richardson plot. Similarly, figure 11 also has two linear regimes for low and high temperature regions. So, the values of σ_o were calculated for two temperature regions. As also shown in figure 11, the values of the $\bar{\Phi}_{bo}$ and A^* were found as 0.264 eV and 7.01×10^{-6} A cm^{-2} K^{-2}, respectively, using equation (10) for low temperature region (80–160 K). The values of these parameters were found as 0.99 eV and 88.12 A cm^{-2} K^{-2}, respectively, for high temperature region (180–340 K). The value of the $A^* = 88.12$ A cm^{-2} K^{-2} for 180–340 K range (for $\sigma_o = 139$ mV) is closer to the theoretical value of 112 A cm^{-2} K^{-2} for n–Si [1, 2].

The R_S of these structures is another parameter that has serious effects on the electrical properties. In addition to the parameters obtained above, we also obtained R_S and Φ_b values using Norde's method [56] for Au/SnS-doped PVC/*n*–Si structures. Norde's function $F(V)$ can be given as follows;

$$F(V) = V/\gamma - \left(\frac{kT}{q}\right)\ln\left(\frac{I(V)}{AA^*T^2}\right) \tag{11}$$

where $I(V)$ is current and γ is an integer which is greater than the n values obtained from the I–V data. From the $F(V)$–V plot, the BH and R_s equations can be determined as follows:

$$\Phi_b = F(V_0) + \frac{V_0}{\gamma} - \frac{kT}{q} \tag{12}$$

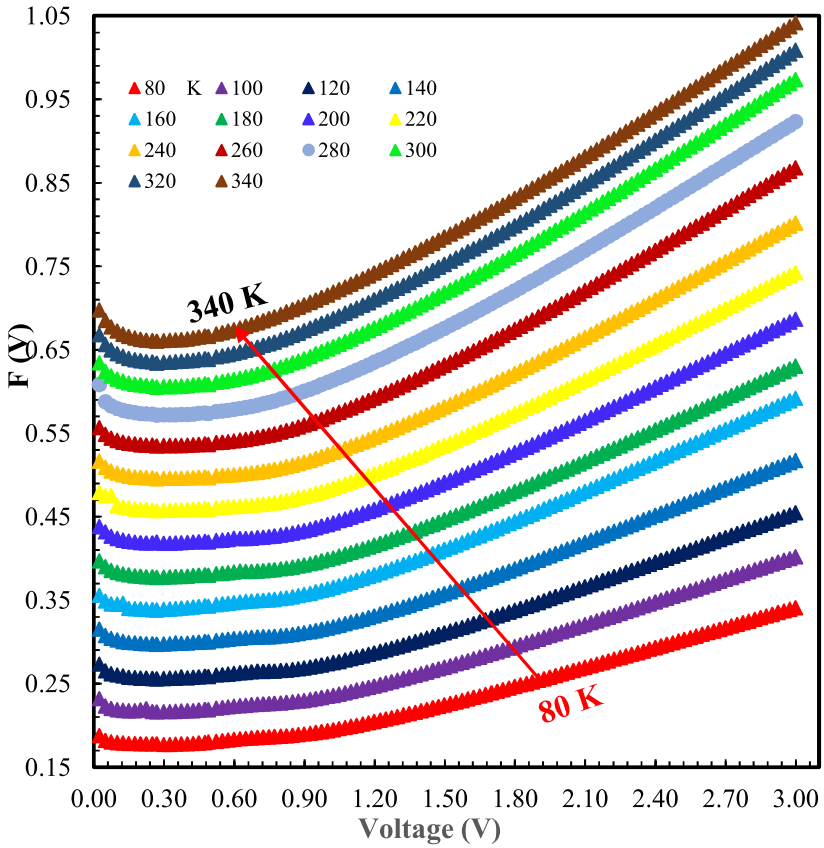

Figure 12. Experimental $F(V)$–V curves of the Au/SnS-doped PVC/n–Si structure obtained using Norde method in the range 80–420 K.

$$R_S = \left(\frac{\gamma - n}{I}\right)\frac{kT}{q} \tag{13}$$

where $F(V_0)$ is the value that corresponds to minimum value of $F(V)$–V plot, similarly V_0 and I is are the bias and current values that correspond to this minimum value of $F(V_0)$, respectively. Figure 12 shows the $F(V)$ versus V curves of the Au/(SnS-doped PVC)/n–Si structures at different-temperatures. Using equations (12) and (13), the Φ_b and R_S values were obtained to be 0.208 eV and 9504.13 Ω at 80 K and 0.719 eV and 258.55 Ω at 340 K, respectively. The obtained Φ_b and R_S values from Norde method are also given in figure 13 and table 1. It is seen that the values Φ_b and R_S obtained using Norde's method are different than their values found on the basis of TE theory. This is partly because this method is applied to all part of the I–V curves whereas only the Rs region is taken into account while using TE theory. That is, the whole portion of the curve under forward bias is taken into consideration in Norde's method; the current varies exponentially in this area. As seen in figure 13 and regarding columns of table 1, Φ_b values calculated with Norde method increase with increasing temperature whereas R_S values decrease. The increase in BH with increasing temperature can be attributed to N_{ss} and cleaning processes of surface. That is, more and more carriers will gain sufficient energy to surmount BH at high temperatures. In the same way, the decrease in R_S values results from increasing number of carriers at high temperatures.

Furthermore, the temperature dependent N_{SS} was determined from I–V data as a function of the energy (E_C-E_{SS}) using Card-Rhoderick method [47]. According to [47], N_{SS} can be written as follows:

$$qN_{SS}(V) = \left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \left(\frac{\varepsilon_s}{W_D}\right)\right] \tag{14}$$

where W_D is the depletion layer width, $n(V)$ is the voltage dependent ideality factor ($n(V) = V/(kT/q)\ln(I/I_0)$), ε_s and ε_i are the dielectric permittivity of the semiconductor and interlayer, and δ is the interfacial layer thickness ($\delta = \varepsilon_i\varepsilon_o A/C_{max}$).

The energy profiles (Ec–Ess) of N_{SS} for each temperature value were obtained using equation (14) and given in figure 14. The increase in N_{SS} from the mid-gap to the bottom of the conduction band is quite noticeable in figure 14, and the values obtained for N_{SS} varied between approximately 2.4×10^{12} eV^{-1} cm^{-2} and 1.93×10^{13} eV^{-1} cm^{-2}. The decrease in N_{SS} with increasing temperature is attributed to large number of electronic charges escaping from these states/traps at sufficiently high temperatures due to high thermal energy [57–59]. According to these experimental results, the existence of (SnS-doped PVC) thin layer between the Au and n–Si

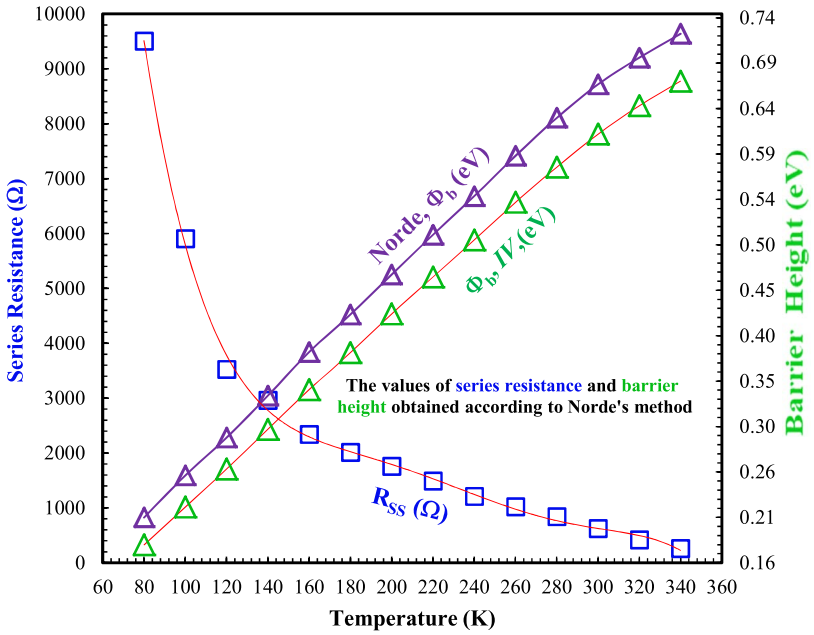

Figure 13. Temperature dependence of the series resistance and barrier height values obtained from the Norde function of the Au/SnS-doped PVC/*n*–Si structure..

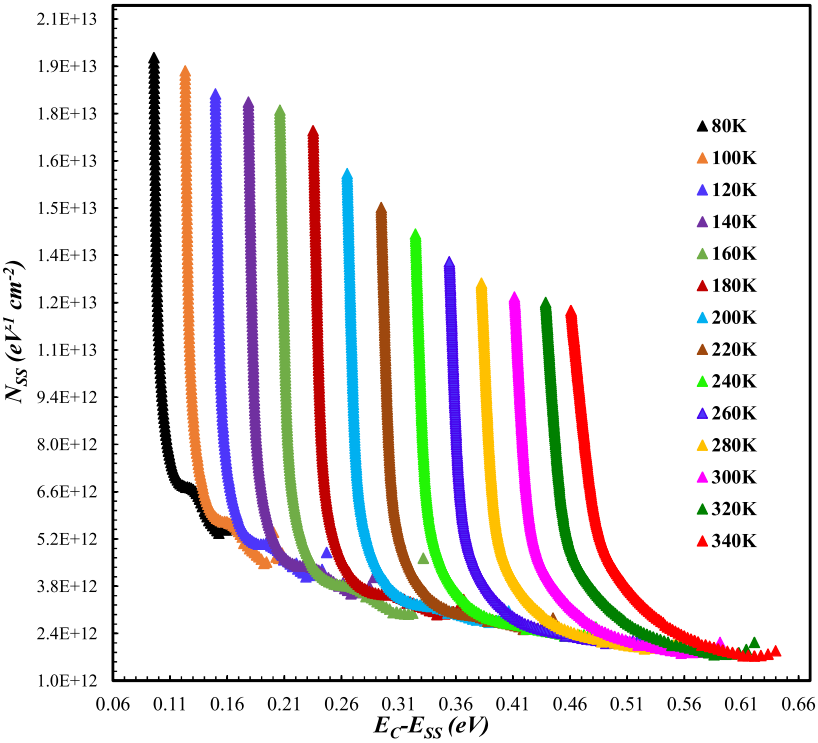

Figure 14. Temperature dependent interface state density (N_{SS}) versus energy profiles (*Ec–Ess*) curves of the Au/SnS-doped PVC/*n*–Si structure.

leads to enhancements for the performance of MS structure regarding lower values of N_{ss} and leakage current and also higher values of BH and RR through passivation of many defects or interface traps.

Conclusion

In this study, the temperature dependent electrical characteristics of Au/(SnS-doped PVC)/*n*–Si structure have been examined using *IV* characteristics in the wide temperature and voltage ranges based on standard TE theory.

Experimental results showed that n decreases with increasing temperature whereas Φ_{bo} increases. In addition, the conventional Richardson plot deviated from the linearity at low temperatures, furthermore the value of A^* was found quite lower than its theoretical value due to the inhomogeneity in the BH at Au/n–Si interface. High values of n for the Au/(SnS-doped PVC)/n–Si structure especially at low temperatures were attributed to the existence of the organic interlayer, the barrier inhomogeneity, and surface-states. Hence, the plots of Φ_{bo} versus n, Φ_{bo} and $(n_{ap}^{-1} - 1)$ versus $(2\,kT)^{-1}$ were drawn to explore barrier inhomogeneity in detail. These plots yielded two distinct linear regimes that corresponded to low temperature (80–160 K) and high temperature (180–340 K) regions. The plot of Φ_{bo} versus $(2\,kT)^{-1}$ yields that values of mean BH ($\bar{\Phi}_{bo}$) as 0.486 and 0.555 eV and standard deviations (σ_o) as 66 mV and 139 mV for the two regions, respectively. Thus, the values of $\bar{\Phi}_{bo}$ and A^* were obtained as 0.264 eV and 7.013 $\times$ 10^{-6} A cm^{-2} K^{-2} (80–160 K) and 0.994 eV and 88.115 A cm^{-2} K^{-2} (180–340 K), respectively, using the plot of $\ln(I_0/T^2)$–$q^2\,\sigma_o^2/2k^2T^2$ versus q/kT. It is clear that this value of A^* (=88.12 A cm^{-2} K^{-2}) obtained for high temperature region is closer to the known theoretical value of 112 A cm^{-2} K^{-2} for n-type Si. Moreover, Norde's method was used to determine the values of R_s and BH, and the results are quite similar to those obtained using the IV method. Finally, the plots of N_{SS} versus (Ec–Ess) were drawn by using Card-Rhoderick method by considering voltage dependence of BH and n. These plots showed that the values of Nss decrease with the increasing temperature. All these results show that CMs in the fabricated Au/(SnS-doped PVC)/n–Si structure can be successfully explained by the double GD of BH around mean BH. In conclusion, (SnS-doped PVC) thin organic interfacial layer at Au/n–Si interface led to improvement of the performance of Au/n–Si structure in terms of low values of N_{ss} and leakage current and also high values of BH and RR through passivation of many defects or interface traps.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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